RCE, 2800

#11

PTO/SB/30 (5/2000)
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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of an utility or plant application filed on or after June 8, 1995.
See The American Inventors Protection Act of 1999 (AIPA).

Application Number	09/967,044
Filing Date	09/28/2001
First Named Inventor	Douglas T. Grider
Group Art Unit	2823
Examiner Name	Julio J. Maldonado
Attorney Docket Number	TI-31118

This is a Request for Continued Examination (REC) under 37 C.F.R. § 1.114 of the above-identified application.
NOTE: 37 C.F.R. § 1.114 is effective on May 29, 2000. If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. § 1.53 (d) (PTO/SB/29) instead of a RCE to be eligible for the patent term adjustment provisions of the AIPA. See Changes to Application Examination and provisional Application Practice, Interim Rule, 65 Fed. Reg. 14865 (Mar. 20, 2000), 1233 Off. Gaz. Pat. Office 47 (Apr. 11, 2000), which established RCE practice.

1 **Submission required under 37 C.F.R. § 1.114**

a ☐ Previously submitted
- i. ☐ Consider the amendments(s)/reply under 37 C.F.R. § 1.116 previously filed on ________.
  (Any unentered amendment(s) referred to above will be entered).
- ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on ________.
- iii. ☐ Other

b ☒ Enclosed
- i. ☒ Amendment/Reply
- ii. ☐ Affidavit(s)/Declaration(s)
- iii. ☐ Information Disclosure Statement (IDS)
- iv. ☐ Other ________

2 **Miscellaneous**

a ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103 (c) for a period of ____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17 (i) required)

b ☐ Other ________

3 **Fees** The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a ☒ The Director is hereby authorized to charge the following fees, or credit any overpayments, to **Deposit Account No. 20-0668, Texas Instruments Incorporated.**
- i. ☒ RCE fee required under 37 C.F.R. § 1.17(e)
- ii. ☒ Extension of time fee (37 C.F.R. §§ 1.136 and 1.17)
- iii. ☐ Other ________

b ☐ Check in the amount of $________ enclosed

c ☐ Payment by credit card (Form PTO-2038 enclosed)

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print / Type)	Peter K. McLarty	Registration No. (Attorney / Agent)	44,923
Signature	[signature]	Date	10/15/2003

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on:

Name (Print or Type)	Ann Trent		
Signature	[signature]	Date	10-15-03

#12/B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Douglas T. Grider	Docket No:	TI-31118
Serial No:	09/967,044	Conf. No:	4815
Examiner:	Julio J. Maldonado	Art Unit:	2823
Filed:	09/28/2001		

For: METHOD FOR TRANSISTOR GATE DIELECTRIC LAYER WITH UNIFORM NITROGEN CONCENTRATION

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 10-15-03.

Ann Trent
Ann Trent

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above identified application, Applicant respectfully submits the following amendments and remarks.

Amendments to the Specification:

None

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A method for forming a MOS transistor gate dielectric layer comprising:

providing a semiconductor substrate;

forming an oxide layer on the semiconductor substrate;

exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

annealing said oxynitride layer in N_2O to form an oxynitride layer with a ~~uniform nitrogen concentration profile~~ a nitrogen concentration with less than 10% variation across the oxide layer.

Claim 2 (original): The method of claim 1 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 – 900 watts.

Claim 3 (original): The method of claim 1 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of 800°C – 1100°C for 10-60 seconds.

Claim 4 (currently amended): A method of forming a MOS transistor comprising:

providing a semiconductor substrate;

forming a gate dielectric layer less than 40 angstroms thick on the semiconductor substrate wherein the gate dielectric layer has a ~~uniform nitrogen concentration~~ nitrogen concentration with less than 10% variation across the gate dielectric layer and ;

forming a conductive layer on said gate dielectric layer,

forming sidewall structures adjacent to said conductive layer; and

forming source and drain regions in the semiconductor substrate adjacent to said sidewall structures.

Claim 5 (currently amended): The method of claim 4 wherein said forming a the gate dielectric layer ~~with a uniform nitrogen concentration~~ comprises:

forming an oxide layer on the semiconductor substrate;

exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

annealing said oxynitride layer in N_2O to form an oxynitride layer with a uniform nitrogen concentration profile.

Claim 6 (original): The method of claim 5 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 – 900 watts.

Claim 7 (original): The method of claim 5 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of 800°C – 1100°C for 10-60 seconds.

Claim 8 (original): The method of claim 4 wherein said uniform nitrogen concentration is greater than 6 atomic percent.

Claim 9 (canceled)

Claim 10 (canceled)

Claim 11 (withdrawn): A MOS transistor, comprising:

providing a silicon substrate;

a gate dielectric layer on the silicon substrate wherein the gate dielectric layer is less than 40 angstroms thick and wherein the gate dielectric layer has a uniform nitrogen concentration;

a conductive layer on the gate dielectric layer;

sidewall structures adjacent to said conductive layer; and

source and drain regions in the silicon substrate adjacent to the sidewall structures.

Claim 12 (withdrawn): The MOS transistor of claim 10 wherein the uniform nitrogen concentration is greater than 6 atomic percent.

Claim 13 (withdrawn): The MOS transistor of claim 12 wherein the uniform nitrogen concentration has a variation of less than 10% across the gate dielectric layer.

Claim 14 (new): A method of forming a MOS transistor comprising:

providing a semiconductor substrate;

forming a gate dielectric layer less than 40 angstroms thick on the semiconductor substrate such that the gate dielectric layer has a nitrogen concentration greater than 6 atomic percent with less than 10% variation across the gate dielectric layer;

forming a conductive layer on said gate dielectric layer,

forming sidewall structures adjacent to said conductive layer; and

forming source and drain regions in the semiconductor substrate adjacent to said sidewall structures.

Claim 15 (new): The method of claim 14 wherein said forming said gate dielectric layer comprises:

forming an oxide layer on the semiconductor substrate;

exposing the oxide layer to a high-density nitrogen plasma to incorporate nitrogen into the oxide layer thereby converting the oxide layer to an oxynitride layer; and

annealing said oxynitride layer in N_2O to form an oxynitride layer with a uniform nitrogen concentration profile.

Claim 16 (new): The method of claim 15 wherein the exposing the oxide layer to a high-density nitrogen plasma comprises a plasma power level of 700 – 900 watts.

Claim 17 (new): The method of claim 16 wherein annealing the oxynitride layer in N_2O comprises rapid thermal annealing at a temperature of 800°C – 1100°C for 10-60 seconds.

Amendments to the Drawings:

None

REMARKS/ARGUMENTS

Claims 1-8 and 14-17 remain in the application for consideration by the Examiner.

An early and favorable action is respectfully requested.

Should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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